

Customer No.: 31561  
Docket No.: 12336-US-PA  
Application No.: 10/710,662

### REMARKS

#### Present Status of the Application

The Office Action rejected all presently-pending claims 1-8, 10-18 and 20. Specifically, the Office Action rejected claims 10-18 and 20 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description. Claims 10-15, 17-18 are rejected under 35 U.S.C. 102(b), as being anticipated by Chakravorty et al.(U.S. Pat. 6,181,569). The Office Action also rejected claims 16 and 20 under 35 U.S.C. 103(a) as being unpatentable over Chakravorty et al. in view of Chi et al. (U.S. Pat. 6,828,211). The Office Action also rejected claims 1-8 under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US Pat. 6,571,485) in view of Chi et al.

In response thereto, Applicant has cancelled claims 11-14 and amended claim 10 to more clearly define the present invention. After entry of the foregoing amendments, claims 1-8, 10, 15-18 and 20 remain pending in the present invention, and reconsideration of those claims is respectfully requested.

#### Claim Rejections under 35 U.S.C. 112, first paragraph

The Office Action rejected claims 10-18 and 20 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description. The office action stated the applicant's disclosure does not have a dielectric layer without any openings to relieve stress from a wafer, and it is not suggested in applicant's drawings nor in the specification.

Applicant explains the limitation "there is no opening formed in the dielectric layer

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"within the first area" is shown in Figs. 3A-3D. In Figs. 3A-3D, the dielectric layer 208 has no opening therein in the first region 204. In addition, the first region 204 is a region for a scribe line, and in practice, circuits, openings and the like would not be formed in this region. Therefore, applicant respectfully submits the claims contains subject matter which was described in the specification in such a way as to reasonably convey to one skilled in the art, at the time the application was filed, has possession of the claimed invention.

**Claim Rejections under 35 U.S.C. 102(b)**

*Claims 10-15, 17-18 are rejected under 35 U.S.C. 102(b), as being anticipated by Chakravorty et al.(U.S. Pat. 6,181,569). In response thereto, Applicant has amended independent claim 10 and canceled claims 11-14, and hereby otherwise traverse the 102(b) rejection of claims 10, 15 and 17-18 because Chakravorty et al. does not teach each and every element recited in these claims.*

The present invention is related to a stress relieving method as amended claim 10 recites:

**Claim 10.** A stress relieving method for a wafer, comprising the steps of:  
providing a wafer with a dielectric layer thereon, wherein the wafer is divided into a first area and a second area such that no circuits are formed within the first area, *the first area comprising a scribe line, the second area comprising a region for forming a die, wherein there is no opening formed in the dielectric layer within the first area;*  
forming a first material layer over the wafer to cover the dielectric layer; and

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*forming a plurality of first openings in the first material layer within the first area. (Emphasis added)*

Applicant respectfully submits Chakravorty fails to teach forming a plurality of first openings in the first material layer within the first area comprising a scribe line as claim 10 recited. The office action stated Chakravorty disclosed the first area comprises a scribe line in Fig. 6. As a matter of fact, Fig. 6 is one of the steps for a chip package process, and the structure shown in Fig. 6 is in the region where the chip 302 is disposed. Please see Fig. 2 and col. 7, lines 45-47, Chakravorty disclosed the reference number 302 refers as a chip while the reference number 303 refers as a scribe line. In addition, the step shown in Fig. 6 is followed Figs. 4-5a, and the chip contact pads are labeled as reference number 304, and obviously, the chip contact pads in Fig. 6 is mis-labeled as reference number 303. Therefore, Fig. 6 of the citation does not show the scribe line, and thus Chakravorty does not teach the feature of forming a plurality of first openings in the first material layer within the first area comprising a scribe line.

In view of the foregoing or other reasons, Applicant respectfully submits Chakravorty fails to teach or suggest every element recited in claim 10. Therefore, after entry of the amendments, Applicant respectfully submits that independent claim 10 patently defines over the prior art reference, and should be allowed. Since independent claim 10 should be allowed over the prior art of record, its dependent claims 15, 17-18 should also be allowed as a matter of law, because the dependent claims contain all features of their respective independent claims 1 and 10. *In re Fine*, 837 F.2d 1071 (Fed.

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Cir. 1988).

**Claim Rejections under 35 U.S.C. 103(a)**

*The Office Action also rejected claims 16 and 20 under 35 U.S.C. 103(a) as being unpatentable over Chakravorty et al. in view of Chi et al. (U.S. Pat. 6,828,211). Applicant respectfully traverses the rejections for at least the reasons set forth below.*

Applicant submits that, as disclosed above, Chakravorty fails to teach or suggest each and every element of claim 10, from which claims 16 and 20 depend. Chi also fails to teach the feature of forming a plurality of first openings in the first material layer within the first area comprising a scribe line. Chi cannot cure the deficiencies of Chakravorty. Therefore, independent claim 10 is patentable over Chakravorty and Chi. For at the least the same reasons, their dependent claims 16 and 20 are also patentable.

*The Office Action also rejected claims 1-8 under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US Pat. 6,571,485) in view of Chi et al. Applicant respectfully traverses the rejections for at least the reasons set forth below.*

The present invention is related to a stress relieving method as amended claim 1 recites:

Claim 1. A stress relieving method for a wafer, comprising the steps of:  
providing a wafer with a dielectric layer thereon, wherein the wafer is divided into a first area and a second area such that at least no circuits are formed on the dielectric

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layer within the first area;

forming a plurality of first openings in the dielectric layer within the first area;  
and

forming a first material layer over the wafer, wherein the upper surface of the first material layer has pits at locations over the first openings, *and the first material layer is a high stress dielectric layer. (Emphasis added)*

The office action stated that Yu et al. disclosed all the claimed subject matter except the feature that the first material layer is a high stress dielectric layer. However, Chi discloses the first material layer is a high stress dielectric in Fig. 8, reference 26. Applicant respectfully disagrees. As a matter of fact, Chi discloses "as shown in FIG 8, the second dielectric layer is preferably *a high-k dielectric material*..... Some promising high-k materials include Al<sub>2</sub>O<sub>5</sub>, Ta<sub>2</sub>O<sub>5</sub> (k.about.25), HfO<sub>2</sub> (k.about.30), . . . etc. with k>20" (see col. 6, lines 24-31). Applicant respectfully submits that Chi teaches the dielectric layer is a high-k dielectric material but not disclose the dielectric layer is a high stress dielectric.

In view of the foregoing or other reasons, Applicant respectfully submits Yu and Chi combined do not teach or suggest each and every element recited in claim 1. Independent claim 1 patently defines over the prior art references, and should be allowed. Since independent claim 1 should be allowed over the prior art of record, its dependent claims 2-8 should also be allowed as a matter of law, because the dependent claims contain all features of their respective independent claim 1.

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**CONCLUSION**

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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